ENSONIQ AudioPCI™ 97
ES1373
Specification

PRELIMINARY

1. INTRODUCTION

AudioPCI 97 is the new ENSONIQ AC97 digital controller which provides the next generation of audio performance to the PC market. AudioPCI 97 is a 5.0 Volt PCI bus compatible device that enables the ENSONIQ SoundScape PCI solution. AudioPCI 97 along with an AC97 CODEC offer the next generation of audio performance in a PC while maintaining full legacy compatibility without old ISA bus solutions. Some of the capabilities of AudioPCI 97 are:

- SoundScape WaveTable synthesizer .
- Full DOS Game Compatibility
- Multiple sample rate support
- PCI Bus Master for fast DMA
- Sounds are stored in Main memory.
- Access to Ensoniq's World Famous Sound Library of over 4000 Sounds
- 3 Stereo inputs and 3 mono inputs can be mixed into the output stream.
- Direct I/O space access of the control registers.
- 100 Pin PQFP {rectangular}
- Digital I/O compatible with consumer mode S/PDIF (out) or I2S (in)
- No ISA bus pins required
- Fully Compliant with PC97 Power Management specification

2. DESIGN CONCEPT

AudioPCI 97 is a PCI bus master and slave device that is best understood by looking at the device as four interactive subsystems: the PCI interface, DMA control, LEGACY functions, and the CODEC.

2.1. PCI Interface

The PCI subsystem is a bus master interface that performs the memory accesses to keep the Audio cache buffers full and empties the A/D Converter (or I2S input) buffer to main memory as required.
The fundamental concept of AudioPCI 97 is that the PCI interface controller has a sufficiently large internal (on-chip) memory cache to meet the memory bandwidth requirements. There is a Sound Cache block of 64 bytes for each of the audio channels. It is the responsibility of the DMA control and the software to keep the buffers full.
All system control registers are accessed via I/O on the PCI bus. AudioPCI 97 uses 16 Long Words in the I/O space for control registers. All registers are read as Long Words. All registers are written in byte word or longword format.

2.2. DMA Control

AudioPCI 97 essentially implements a 3 channel DMA controller. These virtual DMA channels are implemented via the CCB, PCI and Serial interface modules. The Serial interface signals the CCB module when a cache transfer is required (playback or record). The CCB module then signals the PCI module to initiate a bus master data transfer. At this point the CCB and PCI modules will control the data transfer between host system memory and the AudioPCI 97 internal cache.

2.3. LEGACY

The LEGACY subsystem is the circuitry required to perform SoundBlaster, OPL-FM and MPU-401 emulation. Functionally AudioPCI 97 traps on access of the SoundBlaster registers and then issues the appropriate IRQ or SERR command on the PCI bus. AudioPCI 97 handles the Legacy DMA function in a similar fashion. The exact functionality of the block cannot be fully disclosed at this time due to pending patent protection for the application of this technique.

2.4. CODEC

The Codec controller supports any AC97 compliant CODEC. The functionality of the A/D and D/A sections are similar to those found in other standard CODECs. The A/D portion of the Codec is handled as an independent asynchronous event with a DMA buffer control structure. Each time the A/D FIFO is filled, a Bus Master request occurs and the FIFO is transferred to main memory.

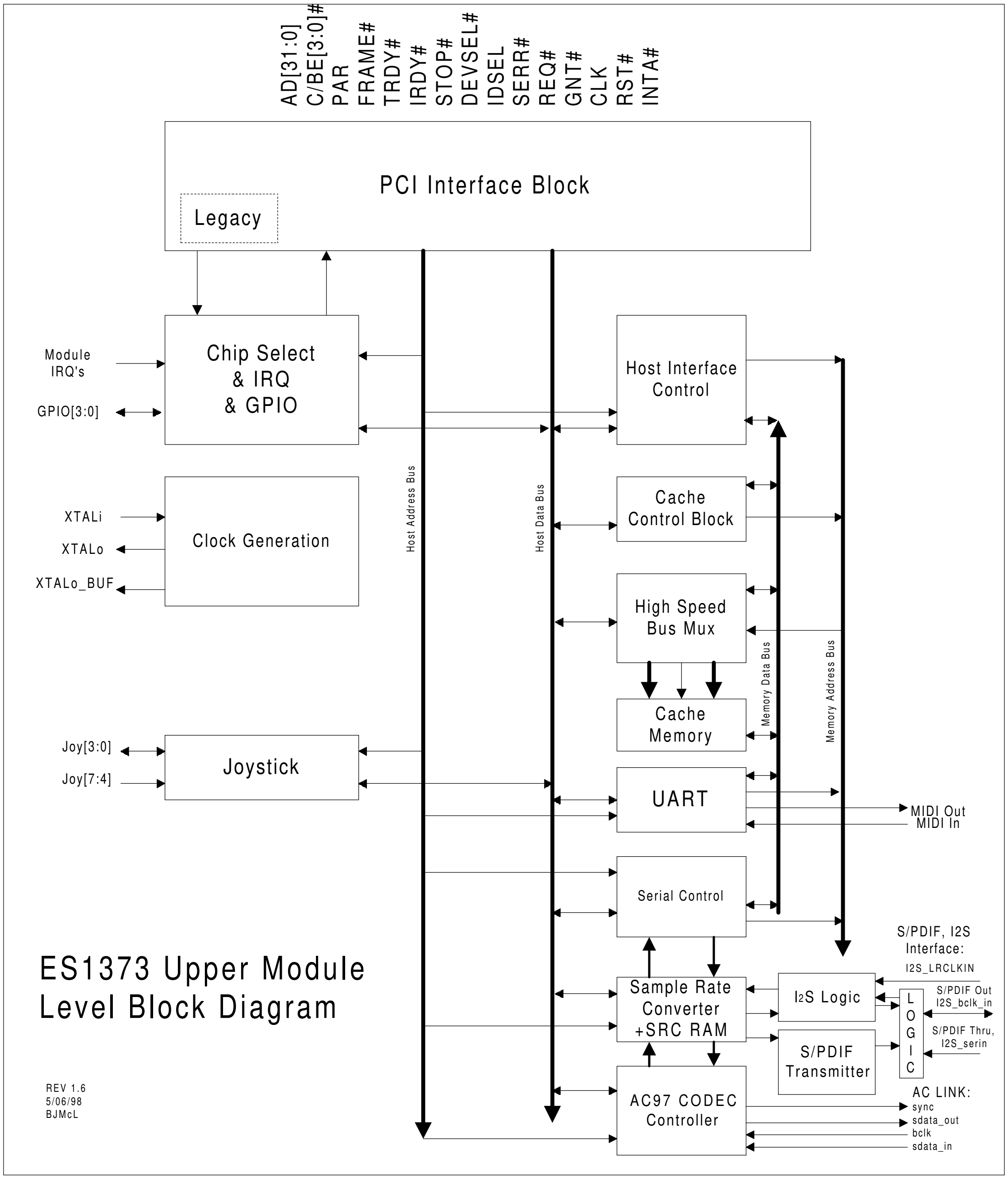
2.5. S/PDIF / I2S Option

In addition to the AC97 CODEC interface, the ES1373 has three pins that are used to support either I2S In { serial format for outboard A/D converters} or S/PDIF Out { Sony/Phillips Digital Interface; to outboard D/A converters or AC3 digital signal processors} .
NOTE: The default mode is for the ES1373 to power up in I2S mode, looking like the ES1371.

2.6. Subsystem ID Override Option

The OEM manufacturer using the ES1373 has the ability to override the default Subsystem ID's.

3. BLOCK DIAGRAM



AD[31:0]
C/BE[3:0]#
PAR
FRAME#
TRDY#
IRDY#
STOP#
DEVSEL#
IDSEL
SERR#
REQ#
GNT#
CLK
RST#
INTA#
PCI Interface Block
Legacy
Module IRQ's
GPIO[3:0]
Chip Select & IRQ & GPIO
Host Interface Control
XTALi
XTALo
XTALo_BUF
Clock Generation
Host Address Bus
Host Data Bus
Cache Control Block
High Speed Bus Mux
Memory Data Bus
Memory Address Bus
Cache Memory
Joy[3:0]
Joy[7:4]
Joystick
UART
MIDI Out
MIDI In
Serial Control
S/PDIF, I2S Interface:
I2S_LRCLKIN
ES1373 Upper Module Level Block Diagram
Sample Rate Converter +SRC RAM
I2S Logic
S/PDIF Out
I2S_bclk_in
LOGIC
S/PDIF Thru,
I2S_serin
S/PDIF Transmitter
REV 1.6
5/06/98
BJMcL
AC97 CODEC Controller
AC LINK:
sync
sdata_out
bclk
sdata_in

4. THE SYSTEM Components

4.1. PCI Interface/LEGACY

The PCI subsystem is a bus master interface that performs the memory accesses to keep the Audio cache buffers full and empties the A/D Converter (or I2S input) buffer to main memory as required.
All system control registers are accessed via I/O on the PCI bus. AudioPCI 97 uses 16 Long Words in the I/O space for control registers. All registers are read as Long Words. All registers are written in byte word or longword format.
The PCI block also includes the functions necessary to provide legacy mode support. This block generates IRQ or SERR# at a specified ADLib access, SoundBlaster access, DMA controller access, IRQ (PIC) controllers access, Microsoft WSS access, or Soundscape access.

4.2. Bus Master Cache Control (CCB)

This block controls the transfer of data between the PCI memory and the internal memory. The Serial block signals when a cache fill/transfer is required in the three memory buffers. The CCB calculates the PCI address from the frame data and issues a command to the PCI interface. When the PCI interface signals that the data is available the CCB channels the data to the proper place in memory. This block is functionally equivalent to a 3 channel DMA controller.

4.3. Serial Interface

This block performs a parallel transfer to/from the internal memory for the record and playback channels respectfully. The record channel source can be either the I2S inputs or the AC97 CODEC ADC serial input signal. This block also signals the CCB block when a cache fill/transfer is required.

4.4. Host Interface

This block arbitrates a PCI access to the internal memory. When the data transfer is complete, it responds with an acknowledge to the PCI interface block. This block provides direct access to the internal memory. It can be used to access the playback/record channels cache, the UART FIFO or the CCB registers.

4.5. CODEC Controller

This block reads/writes configuration data from the host bus to the AC97 CODEC using the serial protocol of the AC97 CODEC. This block also merges the mixed playback channel data into the AC97 CODEC's serial data input, and it retrieves the record channel data from the AC97 CODEC's serial data output.

4.6. IRQ & Chip Select Block

The functions for this block are:

1? Decode the internal address bus to generate chip selects to each block.
2? Contains internal registers whose outputs are control bits used by internal blocks for control/selection.
3? Summarizes all system IRQ's (UART, CODEC, etc.) to generate a single AudioPCI 97 IRQ to the host. This also includes the playback and record DMA channels. Any IRQ masking is performed within the individual blocks except for the CCB block interrupt.

4.7. Joystick

This block contains the logic required to implement the joystick interface for AudioPCI 97.

4.8. UART

This block includes both the transmitter and receiver for the AudioPCI 97 MIDI interface. The UART controller also implements an eight byte FIFO in the internal memory. This FIFO is then accessed through the HOST interface block.

4.9. Sample Rate Converter

This block receives or sends samples from/to the serial interface block for the playback/record channels. The Sample Rate converter block converts two variable input rate playback channels to one fixed rate (48Khz) output channel. It also takes one fixed input rate (48Khz) record channel and converts it to a variable rate output channel. The channels are programmed by writing several ram locations that are a function of the input and output rates. The Sample Rate Converter block has it's own memory section. The Sample Rate Converter memory is accessible only by the Sample Rate Converter block.

The first stage consists of expanding the number of input samples by an integer number (N), up to a maximum of 16, and filling in between the samples with zeros. Then the new samples are filtered by a long 1/32 band FIR filter. In practice, the zeros are not multiplied with their corresponding FIR coefficients. The input samples are fed into an input FIFO and the hardware figures out which FIR coefficient corresponds to each FIFO sample. The starting coefficient and the spacing between successive coefficients are calculated by aligning the FIR filter with a virtual FIFO which is the expanded version of the real FIFO.
The coefficient positions also depend on the third stage in the block diagram, the linear interpolator. This interpolator uses frequency and accumulator registers to interpolate between 2 samples.

4.10. Memory Bus

This pathway is used exclusively to transfer data between the internal sound cache memory and the various sub-systems. The access priority for this bus is (highest to lowest):

Cache Control block
Host Interface
UART Interface
Serial Interface

4.11. Internal Memory

There are two separate sections of memory in AudioPCI 97. One section is allocated as a cache for the playback and record channels and also as a FIFO for the UART. The other section is allocated to the Sample Rate Converter module and is used as a cache for sample rate conversion and also as control register space for the playback and record channels in the sample rate converter.

The internal memory for the sound cache in AudioPCI 97 is organized as 4 blocks of 64 bytes each. Each block is divided into 4 pages of 16 bytes each (4 longwords). Memory can be accessed as longwords only. In order to access a specific page of memory the memory page register must first be setup for the specific page to be accessed. The first three blocks of memory contain the 3 circular buffers for the 2 playback channels and the record channel. The last block contains the frame information for the playback and record channels and also includes the UART FIFO. The memory block and page organization is shown below :

Block	Page	Higher	Address	Lower
0 - DAC 1	0000	DAC1 sample bytes 15 - 0	Lower half buffer	
	0001	DAC1 sample bytes 31 - 16		
	0010	DAC1 sample bytes 47 - 32	Upper half buffer	
	0011	DAC1 sample bytes 63 - 48		
1 - DAC2	0100	DAC2 sample bytes 15 - 0	Lower half buffer	
	0101	DAC2 sample bytes 31 - 16		
	0110	DAC2 sample bytes 47 - 32	Upper half buffer	
	0111	DAC2 sample bytes 63 - 48		
2 - ADC	1000	ADC sample bytes 15 - 0	Lower half buffer	
	1001	ADC sample bytes 31 - 16		
	1010	ADC sample bytes 47 - 32	Upper half buffer	
	1011	ADC sample bytes 63 - 48		
3 - Frame/UART	1100	DAC1, DAC2 frame information (see register descriptions)		
	1101	ADC frame information (plus 2 open longwords)		
	1110	UART fifo (only bits 8 - 0 of each longword are used)		
	1111	UART fifo		

The internal memory organization for the Sample Rate Converter in AudioPCI 97 is shown below. The memory is accessed through the Sample Rate Converter interface register located at address 10H.

Loc(hex)	Fifo Ram 128x16
0	PLAY 1 Left
10	PLAY 1 Right
20	PLAY 2 Left
30	PLAY 2 Right
40	REC Left
56	REC Right
6c	Volume Reg Rec
70	PLAY 1 Regs
74	PLAY 2 Regs
78	REC Regs
7c	Volume Reg Play

PLAY/REC Registers

	15	14–10	9–4	3–0
0	SMF	TRUNC_START	N	HSTART

	15–10	9–8	7–0
1	VF.I	0	AC.I

	15	14–0
2	0	AC.F
3	0	VF.F

Volume Registers

		15–13	12–8	7–0
Rec Left	6c	0	REC.N (copy)	0
Rec Right	6d	0	REC.N (copy)	0
	6e	Unused		
	6f	Unused		

		15	14–12	11–0
Play 1 L	7c	SGN	P1.VOL.I	P1.VOL.F
Play 1 R	7d	SGN	P1.VOL.I	P1.VOL.F
Play 2 L	7e	SGN	P2.VOL.I	P2.VOL.F
Play 2 R	7f	SGN	P2.VOL.I	P2.VOL.F

Sample Rate Converter Interface

31–25	24	23	22	21	20	19	18–16	15–0
RAM ADDR	WE	BUSY	DIS	DP1	DP2	DREC	unused	RAM DATA

4.12. Digital Output

The digital output interface takes playback and record channel samples from the Sample Rate Converter and Codec Controller block and assembles and transmits a frame of digital data in accordance with the IEC 958 consumer mode speci.fication. Mode 0 is used as the Channel Status data format, and it defaults to 2-channel general format, 48kHz sampling frequency, Level II clock accuracy, and no user- data and validity bits. The channel status word for the left and right channels is identical. The first 32 bits of the channel status word are reprogrammable via the Channel Status Register.

Mixing of the record channel audio with the playback audio is optional and is set by programming the proper control register in the IRQ and Chip Select block. There is a one-sample-period latency in the transmitted data.

4.13. User Definable Subsystem Vendor ID and Subsystem ID

This method allows direct PCI Configuration writes to the PCI Configuration Space's Subsystem Vendor ID (WORD @ 2Ch) and Subsystem ID (WORD @ 2Eh) ONLY when a proprietary LOCK in the device specific PCI Configuration Space area is unlocked. The LOCK is implemented in the form of a 1-byte value written to the device specific register at address 40h (SubSysID_wen).

The 1373 device powers-up/resets with Subsystem Vendor ID = ENSONIQ ID (1274h), and the Subsystem ID = 1371h. The device specific register (SubSysID_wen @40h) is initialized to 00h which disables Subsystem writes.

As long as the SubSysID_wen byte is NOT EQUAL TO EAh, the Subsystem Vendor ID and Subsystem ID cannot be changed. When the SubSysID_wen byte is set to EAh, the Subsystem Vendor ID and Subsystem ID values can be modified by PCI Configuration Space writes.
(Note: that the BIOS in control may write these items as WORD, DWORD, or even BYTE.)

The SubSysID_wen byte is a PCI Configuration Space byte at location 40h in the device specific area which is defined as 40h through FFh.

5. PCI Data Transfers

The internal control registers of the AudioPCI 97 Chip and the AC97 CODEC are accessed via 16 Long Words in PCI direct I/O space. These registers are always read as 32 bit longwords but can be written as bytes, words or longwords.
PCI bus mastering is used to transfer audio data between system memory and AudioPCI 97 internal memory. The internal Cache Control Block and the PCI Interface control these transfers. Only burst read/write transfers are allowed. All data transfers are 8 Long Word burst transfers.

5.1. Audio Read Transfers

The CCB requests a read data transfer from the PCI interface block (PCIB). The PCIB arbitrates for the PCI bus and initiates an 8 long word read starting at the system address specified by the CCB in the read request. When the data is acquired, the PCIB signals the CCB to begin moving the data to internal memory. The CCB performs any byte alignment required and writes the data to the appropriate buffer in the internal memory. The CCB will complete the current transfer request and then proceed to the next highest priority request.

5.2. Audio Write Transfers

The CCB will first write up to 8 long words into the intermediate PCI buffer. The CCB will then request a write transfer from the PCIB to main memory and specify the starting address of the transfer. The PCIB arbitrates for the PCI bus and transfers 8 Long Words into system memory. Eight Long words will always be transferred during this operation.

6. PCI CONFIGURATION SPACE

The following information is the PCI configuration space for the AudioPCI 97 chip. All bits not specifically mentioned below are zero and read only.

Vendor ID — Address 00H

Addressable as word
Power on reset value 1274H — Configuration Space

Bit(s)	R/W	Name	Data Value
15:0	R	VENDOR ID	1274H

Device ID — Address 02H

Addressable as word
Power on reset value 1373H — Configuration Space

Bit(s)	R/W	Name	Data Value
15:0	R	DEVICE ID	1371H

Command — Address 04H

Addressable as word
Power on reset value 0000H — Configuration Space

Bit(s)	R/W	Name	Data Value
15:10	R	RESERVED	These bits are reserved and always read back as zeros.
9	R	ZERO	This command bit is not implemented and always reads back as zero.
8	R/W	SERR#_EN	Enable bit for SERR# driver. 0 - SERR# driver disabled. 1 - SERR# driver enabled.
7:3	R	ZERO	These command bits are not implemented and always read back as zeros.
2	R/W	PCI_MASTER	PCI Bus Master enable bit. This bit controls a device's ability to act as a PCI Bus Master. The ES1371 can act as a bus master. 0 - PCI Bus Mastering disabled. 1 - PCI Bus Mastering enabled.
1	R	ZERO	This command bit is not implemented and always reads back as zero.
0	R/W	IO_ACCESS	I/O Space access bit. This bit controls whether the device can be accessed in I/O space. The ES1371 is accessed in this space. 0 - I/O Space access disabled. 1 - I/O space access enabled.

Status — Address 06H

Addressable as word
Power on reset value x610H — Configuration Space

Bit(s)	R/W	Name	Data Value
15	R	PARITY	Parity Error status bit. 0 - No Parity error. 1 - Parity error detected.
14	R	SERR#	SERR# PCI bus signal active status bit. This bit will be set if the AudioPCI 97 ASIC is asserting the PCI SERR# signal. 0 - SERR# signal inactive. 1 - SERR# signal active.
13	R	MASTER-ABORT	Master Abort status bit. This bit will be set whenever a AudioPCI 97 ASIC bus mastering transaction has been terminated by a Master-Abort.
12	R	TARGET-ABORT	Target Abort status bit. This bit will be set whenever a AudioPCI 97 ASIC bus mastering transaction has been terminated by a Target-Abort.
11	R	ZERO	This status bit is not implemented and always reads back as zero.
10:9	R	DEVSEL#	DEVSEL# timing. These status bits encode the timing of the PCI DEVSEL# signal. AudioPCI 97 implements the slow timing mode. 00 - Fast 01 - Medium 10 - Slow 11 - Reserved
8:5	R	ZERO	These status bits are not implemented and always read back as zeros.
4	R	CAPABILITIES	Indicates support for ACPI. The AudioPCI 97 ASIC does support ACPI so this bit is set to a one.
3:0	R	ZERO	These status bits are reserved and always read back as zeros.

Class Code & Revision ID — Address 08H

Addressable as long word

Power on reset value 04010000H — Configuration Space

Bit(s)	R/W	Name	Data Value
31:8	R	CLASS CODE	040100H (Multimedia Audio device)
7:0	R	REVISION ID	04H

Cache Line Size — Address 0CH

Addressable as Byte

Power on reset value 00H — Configuration Space

Bit(s)	R/W	Name	Data Value
7:0	R	CACHE LINE SIZE	00H

Latency Timer — Address 0DH

Addressable as byte

Power on reset value xxH — Configuration Space

Bit(s)	R/W	Name	Data Value
7:3	R/W	LATENCY	Latency Timer specified in PCI bus clocks.
2:0	R	ZERO	0H

Header Type — Address 0EH

Addressable as byte

Power on reset value 00H — Configuration Space

Bit(s)	R/W	Name	Data Value
7:0	R	HEADER TYPE	00H

BIST — Address 0FH

Addressable as byte

Power on reset value 00H — Configuration Space

Bit(s)	R/W	Name	Data Value
7:0	R	BIST	00H

Base Address — Address 10H

Addressable as long word

Power on reset value xxxxxxxxH — Configuration Space

Bit(s)	R/W	Name	Data Value
31:6	R/W	BASE ADDRESS	Variable
5:1	R	ZERO	00H (address 64 byte aligned)
0	R	ONE	1H

Base Address — Address 14, 18, 1C, 20, 24H

Addressable as long word

Power on reset value 00000000H — Configuration Space

Bit(s)	R/W	Name	Data Value

31:0	R	Not implemented	00000000H

Cardbus CIS Pointer — Address 28H

Addressable as long word
Power on reset value 00000000H — Configuration Space

Bit(s)	R/W	Name	Data Value
31:0	R	Not implemented	00000000H

Subsystem Vendor ID — Address 2CH

Addressable as word
Power on reset value 1274H — Configuration Space

Bit(s)	R/W	Name	Data Value
15:0	R	SUBSYSTEM VENDOR ID	1274H
	W	SUBSYSTEM VENDOR ID	Can be written only if SubsysID register (40h) is set to EAh.

Subsystem ID — Address 2EH

Addressable as word
Power on reset value 1371H — Configuration Space

Bit(s)	R/W	Name	Data Value
15:0	R	SUBSYSTEM ID	1371H
	W	SUBSYSTEM ID	Can be written only if SubsysID register (40h) is set to EAh.

Expansion ROM Address — Address 30H

Addressable as long word
Power on reset value 00000000H — Configuration Space

Bit(s)	R/W	Name	Data Value
31:0	R	EXP ROM ADDR	00000000H

Capabilities Pointer — Address 34H

Addressable as long word
Power on reset value DCH — Configuration Space

Bit(s)	R/W	Name	Data Value
7:0	R	CAP_PTR	DCH - Pointer to first entry of capabilities list in configuration space

Interrupt Line — Address 3CH

Addressable as byte
Power on reset value xxH — Configuration Space

Bit(s)	R/W	Name	Data Value
7:0	R/W	INTERRUPT	Variable

Interrupt Pin — Address 3DH

Addressable as byte
Power on reset value 01H — Configuration Space

Bit(s)	R/W	Name	Data Value
7:0	R	INTERRUPT PIN	01H

Min_Gnt — Address 3EH

Addressable as byte

Power on reset value 0CH — Configuration Space

Bit(s)	R/W	Name	Data Value
7:0	R	MIN_GNT	0CH

Max_Lat — Address 3FH

Addressable as byte

Power on reset value 80H — Configuration Space

Bit(s)	R/W	Name	Data Value
7:0	R	MAX_LAT	80H

SubSysid_wen — Address 40H

Addressable as byte

Power on reset value 00H — Configuration Space

Bit(s)	R/W	Name	Data Value
7:0	R/W	SUBSYSID_WEN	00H - SUBSYSTEM ID and SUBSYSTEM VENDOR ID writes disabled. EAH - SUBSYSTEM ID and SUBSYSTEM VENDOR ID writes enabled. Note: This register always reads back as 00H.

Capabilities Identifier — Address DCH

Addressable as byte

Power on reset value 01H — Configuration Space

Bit(s)	R/W	Name	Data Value
7:0	R	CAP_ID	01H - Indicates Power Management Capability

Next Item Pointer — Address DDH

Addressable as byte

Power on reset value 00H — Configuration Space

Bit(s)	R/W	Name	Data Value
7:0	R	Next_Item_Ptr	00H - Indicates last entry in capabilities list

Power Management Capabilities - PMC — Address DEH

Addressable as word - Read Only

Power on reset value 6C31H — Configuration Space

Bit(s)	R/W	Name	Data Value
15:11	R	PME_Support	0DH - Determines level from which PME# can be asserted
10	R	D2_Support	1H - D2 is supported
9	R	D1_Support	0H - D1 is not supported
8:6	R	Reserved	0H
5	R	DSI	1H - Device Specific Initialization Required
4	R	AUXPWR	1H - Auxiliary power required for PME generation
3	R	PMECLK	0H - PCI clock is not required for PME# generation
2:0	R	Version	1H - Indicates conformance to the PCI Power Management 1.0 Specification

Power Management Control/Status - PMCSR   Address E0H
Addressable as byte, word or long word
Power on reset value 00000001H   Configuration Space

Bit(s)	R/W	Name	Data Value
15	R/W clear		PME_Status Set if PME# condition exists regardless of state of PME_En bit. A write of a 1 to this bit clears the PME condition.
14:13	R	Not Implemented	0H -Data Field not implemented, therefore data scale read only
12:9	R	Not Implemented	0H -Data Field not implemented, therefore data select read only
8	R/W	PME_En	Enables the assertion of the PME# pin
7:2	R	Reserved	00H
1:0	R/W	PowerState	00 - D0 01 - D1 10 - D2 11 - D3

Whenever this register is written such that the value of the Power State bits change, an interrupt will be generated. This will appear on the INTA# pin if the PWRINTEN bit is set in the Interrupt Control Register. The interrupt is cleared by writing the CURPDLEV bits in the interrupt control register to equal the value of the Power State bits.

7. REGISTER MAP

All Control registers in AudioPCI 97 are addressed in the direct PCI I/O space. There are control registers for each of the major blocks of the AUDIOPCI system. The memory map is shown below:

AudioPCI 97 Memory Map

Base Address	Upper Address	Module
00H	07H	Interrupt/Chip Select
08H	0BH	UART
0CH	0FH	Host Interface - Memory Page
10H	13H	Sample Rate Converter
14H	17H	CODEC
18H	1BH	LEGACY
1CH	1FH	Channel Status Register
20H	2FH	Serial Interface
30H	3FH	Host Interface - Memory

7.1. IRQ & Chip Select Block

The IRQ/Chip Select block contains two 32 bit registers. The first register is the control register which can be read and written. The second register is the status register which is a read only register, with the exception of 3 bits which serve double duty as 3 additional control bits that can be written to. The control registers includes bits for module enables, interrupt control, general purpose I/O pins and power management functions.

Interrupt/Chip Select Control Register   Address 00H
Addressable as byte, word, longword
Power on reset value FCx0C0F00H   Direct Mapped

Bit(s)	R/W	Name	Function
31	R/W	BYPASS_P1	Bypass the Sample Rate Converter and feed the CODEC directly 0- Normal Mode, Playback Channel Type 1 1- Bypass.
30	R/W	BYPASS_P2	Bypass the Sample Rate Converter and feed the CODEC directly 0- Normal Mode, Playback Channel Type 2 1- Bypass.
29	R/W	BYPASS_R	Bypass the Sample Rate Converter and feed the CODEC directly 0- Normal Mode, Record Channel 1- Bypass.

28 R/W TEST_BIT Set during test to load the frame counter with a value of 2 to verify proper generation of the beginning-of- block preamble. Must be set to 0 for normal operation.
27 R/W RECEN_B Bit to enable or disable the mixing of the record channel audio with the playback audio for inclusion into the digital output data. 0 - Record data is mixed with playback data 1 - No record data is mixed with playback data
26 R/W SPDIFEN_B Reset to switch digital output mux to “THRU” mode. In this mode, any input at input pin SPDIF_THRU is passed through unchanged. 0 - SPDIF_OUT = SPDIF_THRU 1 - SPDIF_OUT = internal SPDIF frame data.
25:24 R/W JOY_ASEL[1:0] These two bits are dedicated to Dave Sowa and will map the joystick port to 4 different base addresses as follows: 00 - Joystick base address $200 01 - Joystick base address $208 10 - Joystick base address $210 11 - Joystick base address $218
23:20 R GPIO_IN[3:0] These bits will read the current value on the GPIO [3:0] pins.
19:16 R/W GPIO_OUT[3:0] These bits when set low will set the corresponding GPIO output low. If these bits are set high then the GPIO pads will be high or they can be used as inputs.
15 R/W MSFMTSEL This bit selects the MPEG serial data format. 0 - SONY (lrclk high = left channel ; data left justified) 1 - I2S (lrclk low = left channel ; data 1 bit clock delayed)
14 R/W SYNC_RES This bit is used to generate a Warm AC97 Reset as described in section 5.2.1.2. of the Audio Codec 97 specification.
13 R/W ADC_STOP This bit when set high will prevent the CCB module from doing a record channel PCI transfer. 0 - CCB will transfer record information. 1 - CCB will not transfer record information.
12 R/W PWR_INTRM This bit selects is the interrupt mask bit for detecting changes in the power management level. 0 - Power level change interrupts are disabled. 1 - Power level change interrupts are enabled.
11 R/W M_CB This bit selects either I2S or the CODEC ADC as the source for the record channel in the serial module. 0 - CODEC ADC is record channel source. 1 - I2S is record channel source.
10 R/W CCB_INTRM This bit is the interrupt mask bit for the CCB module voice interrupts. 0 - CCB voice interrupts are disabled. 1 - CCB voice interrupts are enabled.
9:8 R/W PDLEV[1:0] Current power down level. These bits reflect the power down level the part is currently programmed to. When the Power State bits programmed in configuration space differs from these bits, an interrupt is generated. The ISR should program this to equal the value in configuration space in order to clear the interrupt. 00 - D0 01 - D1 10 - D2 11 - D3
7 R/W BREQ This bit controls access to the internal memory. It is for test purposes only. If this bit is ever set high it will prevent the CCB, Serial, UART and HOSTIF modules from accessing the memory. 0 - Memory bus request disabled (power on state) 1 - Memory bus request enabled (disables memory access)
6 R/W DAC1_EN This bit enables the DAC1 playback channel (CODEC FM DAC). To restart a channel that had stopped, this bit must be reset low and then set high. 0 - DAC1 playback channel disabled 1 - DAC1 playback channel enabled
5 R/W dac2_en This bit enables the DAC2 playback channel (CODEC DAC). To restart a channel that had stopped, this bit must be reset low and then set high. 0 - DAC2 playback channel disabled 1 - DAC2 playback channel enabled
4 R/W adc_en This bit enables the ADC playback channel (CODEC ADC). To restart a channel that had stopped, this bit must be reset low and then set high. 0 - ADC record channel disabled 1 - ADC record channel enabled
3 R/W uart_en This bit enables UART module operation. 0 - UART disabled 1 - UART enabled
2 R/W jystk_en This bit enables Joystick module operation. 0 - Joystick disabled 1 - Joystick enabled
1 R/W XTALCKDIS Xtal Clock Disable. This bit when set high will shut down the crystal clock input to all internal modules. 0 - Xtal Clock enabled. 1 - Xtal Clock Disabled.
0 R/W PCICLKDIS PCI Clock Disable. This bit when set high will shut down the PCI clock input to all internal modules except the PCI module and the Interrupt/Chip Select module. 0 - PCI Clock Enabled 1 - PCI Clock Disabled

Interrupt/Chip Select Status Register — Address 04H

Addressable as longword only

Power on reset value 7F080EC0H — Direct Mapped

Bit(s)	R/W	Name	Function
31	R	intr	This bit is the summary interrupt bit. 0 - No interrupt pending 1 - Interrupt from PLAYBACK1, PLAYBACK2, RECORD, UART, CCB or power management has occurred.
30:24	R	ONES	These bits always read back as ones.
23:20	R/W	GPIO Int Enable	These bits are used to enable the edge triggered interrupts 0 - Interrupt Enabled for corresponding GPIO bit 1 - Interrupt Disabled, for corresponding GPIO bit. Any logic level edge transition will generate an interrupt
19	R	ONE	This bit always reads back as one.
18	R/W	ENABLE_SPDIF	This bit is used to enable the S/PDIF circuitry 0 - S/PDIF, DISABLED, Default state after reset 1 - S/PDIF, Enabled
17	R/W	TEST_SPDIF	This bit is used to put the S/PDIF module in “test_mode”. 0 - Test Mode, DISABLED, Default state after reset 1 - Test_Mode, Enabled
16	R/W	TEST_MODE	This bit is used to put the ASIC in “test_mode”. 0 - Test Mode, DISABLED, Default state after reset 1 - Test_Mode, Enabled
15:12	R	GPIO_INT	These bits are used to indicate that a GPIO interrupt has occurred 0 - NO interrupt pending for corresponding GPIO pin 1 - Interrupt pending for corresponding GPIO pin
11:9	R	ONES	These bits always read back as ones.
8	R	SYNC_ERR	This bit indicates a synchronization error has occurred in the CODEC interface module. 0 - CODEC synchronization error has not occurred. 1 - CODEC synchronization error has occurred.
7:6	R	vOIcE[1:0]	These bits are the voice code from the CCB module. These bits are only valid if the CCB interrupt bit (mccb) is high. 00 - PLAYBACK1 01 - PLAYBACK2 {SoundBlaster} 10 - RECORD 11 - Undefined
5	R	MPWR	This bit indicates whether a power level interrupt has occurred. 0 - No Power Level interrupt. 1 - Power Level interrupt pending.
4	R	mccb	This bit is the masked CCB interrupt bit. A CCB interrupt will occur if a PCI bus abort condition occurs during a voice buffer transfer. The CCB interrupt is masked with the CCB interrupt mask bit (ccb_intrm) in the control register. 0 - No CCB interrupt 1 - CCB interrupt pending
3	R	uart	This bit is the UART interrupt bit. 0 - No UART interrupt 1 - UART interrupt pending
2	R	dac1	This is the DAC1 playback channel interrupt bit. 0 - No DAC1 channel interrupt 1 - DAC1 channel interrupt pending
1	R	dac2	This is the DAC2 playback channel interrupt bit. 0 - No DAC2 channel interrupt 1 - DAC2 channel interrupt pending
0	R	adc	This is the ADC record channel interrupt bit. 0 - No ADC channel interrupt 1 - ADC channel interrupt pending

7.2. UART

The UART contains three 8 bit registers. The data register can be read or written and is used to receive or transmit MIDI information. The second register is a 8 bit control register which is write only. The third register is a 8 bit status register which is read only.

UART Data Register — Address 08H

Addressable as byte only

Power on reset value ??H — Direct Mapped

Bit(s)	R/W	Name	Function
7:0	R/W	data[7:0]	The UART data register provides access to MIDI serial data

input/output.

UART Status Register Address 09H
Addressable as byte only
Power on reset value 00H Direct Mapped

Bit(s)	R/W	Name	Function
15	R	rxint	This bit is the UART receiver interrupt bit. 0 - No UART receiver interrupt 1 - UART receiver interrupt pending
14:11	R	zero	These bits always read back as zeros to allow for soundscape detection.
10	R	txint	This bit is the UART transmitter interrupt bit 0 - No UART transmitter interrupt 1 - UART transmitter interrupt pending
9	R	txrdy	This bit is the UART transmitter ready bit. 0 - UART transmitter not ready 1 - UART transmitter ready
8	R	rxrdy	This bit is the UART receiver ready bit. 0 - UART receiver not ready 1 - UART receiver ready

UART Control Register Address 09H
Addressable as byte only
Power on reset value 00H Direct Mapped

Bit(s)	R/W	Name	Function
15	W	rxinten	This bit is the UART receiver interrupt enable bit. 0 - UART receiver interrupts disabled 1 - UART receiver interrupts enabled
14:13	W	txinten[1:0]	These two bits are the control bits for the UART transmitter operation. 00 - 01 - Txrdy interrupts enabled 10 - 11 -
12:10		undefined	These bits are undefined
9:8	W	cntrl[1:0]	These two bits are the control bits for the UART. 00 - 01 - 10 - 11 - Software Reset

UART Reserved Register Address 0AH
Addressable as byte only
Power on reset value 00H Direct Mapped

Bit(s)	R/W	Name	Function
7:1		undefined	These bits are undefined.
0	R/W	test_mode	This bit enables the UART test mode. When the test mode bit is set the UART clock is switched to the PCI bus clock. The faster clock reduces the size of the test vectors and also shortens the run time of the test vectors. The power up state is normal mode enabled. 0 - Normal mode enabled. 1 - UART test mode enabled.

7.3. Host Interface - Memory Page

The memory page register is a four bit register used to access one of 16 memory pages within the AUDIOPCI chip. This register can be read or written but any unused bits are undefined on read back.

Memory Page Register Address 0CH
Addressable as byte, word, longword
Power on reset value ???????0H Direct Mapped

Bit(s)	R/W	Name	Function
31:4		undefined	These bits are undefined.
3:0	R/W	memory page	These bits select what memory page will be accessed. Each memory page is 16 bytes and is addressed from 30H - 3FH.

7.4. *Sample Rate Converter*

This block receives or sends samples from/to the serial interface block for the playback/record channels. It also provides the necessary sample rate conversion for the AC97 CODEC. The Sample Rate Converter block contains one 32 bit register. This register is used to read/write the Sample Rate Converter FIFO/Control RAM.

Sample Rate Converter Interface Register Address 10H

Addressable as longword

Power on reset value 00000000H Direct Mapped

Bit(s)	R/W	Name	Function
31:25	R/W	SRC_RAM_ADR	These bits are the address of the Sample Rate Converter RAM location to be accessed.
24	R/W	SRC_RAM_WE	This bit is the read/write control bit for accessing the Sample Rate Converter RAM.
23	R	SRC_RAM_BUSY	This bit when high indicates the Sample Rate Converter is accessing the RAM. This bit will be set within 3 PCI clocks after accessing this register. This bit will be Reset when the requested read/write RAM operation has been completed.
22	R/W	SRC_DISABLE	This is the enable bit for the Sample Rate Converter. 0 - Sample Rate Converter enabled. 1 - Sample Rate Converter disabled.
21	R/W	DIS_P1	This bit when high will disable Playback channel 1 from updating the accumulator. 0 - Playback channel 1 accumulator update enabled. 1 - Playback channel 1 accumulator update disabled.
20	R/W	DIS_P2	This bit when high will disable Playback channel 2 from updating the accumulator. 0 - Playback channel 2 accumulator update enabled. 1 - Playback channel 2 accumulator update disabled.
19	R/W	DIS_REC	This bit when high will disable Record channel from updating the accumulator. 0 - Record channel accumulator update enabled. 1 - Record channel accumulator update disabled.
18:16	R/W	UNDEFINED	These bits are undefined.
15:0	R/W	SRC_RAM_DATA	These bits are the value of the RAM to be read/written from /to the RAM at the location pointed to by the SRC_RAM_ADR address pointer above.

7.5. *CODEC Interface*

The CODEC interface register is a 32 bit register that provides access to the AC97 CODEC control registers. This register is a pseudo read/write and must be accessed as a longword. A write to this register will initiate a CODEC register read/write operation. A read from this register is used to read a CODEC register that was initiated by a previous write to the CODEC interface register.

CODEC Write Register Address 14H

Addressable as longword

Power on reset value 00000000H Direct Mapped

Bit(s)	R/W	Name	Function
31:24	W	ZERO	These bits are always zeros.
23	W	PIRD	AC97 Codec register read/write control bit 0 - Write AC97 CODEC register. 1 - Read AC97 CODEC register.
22:16	W	PIADD	These bits are the address of the AC97 CODEC register to be read/written.

15:0 W PIdat These bits are the data value to be written into the AC97 CODEC register. Set to zero for a AC97 CODEC register read.

CODEC Read Register Address 14H
Addressable as longword
Power on reset value 00000000H Direct Mapped

Bit(s)	R/W	Name	Function
31	R	RDY	This bit when high indicates that this register contains valid read data from the AC97 CODEC register file.
30	R	WIP	This bit when high indicates that a register read/write to the AC97 CODEC is in progress. 0 - AC97 CODEC register interface inactive. 1 - AC97 CODEC register access in progress.
29:24	R	ZERO	These bits always read back as zeros.
23	R	PORD	AC97 Codec register read/write control bit 0 - Write AC97 CODEC register. 1 - Read AC97 CODEC register.
22:16	R	POADD	These bits are the address of the AC97 CODEC register for the read register operation.
15:0	R	POdat	These bits are the data value read from the AC97 CODEC register at the above address.

7.6. Legacy

The Legacy register is a 32 bit register that performs both control and status functions. Basically the lower word functions as the status register and the upper word functions as the control register. The only exception to this is bit zero which is a control bit for a write and a status bit for a read.

Legacy Control/Status Register Address 18H
Addressable as byte, word, longword
Power on reset value 00?????0000000001111?????????0?b Direct Mapped

Bit(s)	R/W	Name	Function
31	R/W	jfast	This bit selects fast (vs ISA) joystick timing. 0 - ISA joystick timing 1 - FAST joystick timing
30	R/W	hib	This bit is the host interrupt blocking enable bit (DMA config bit must be set) to prevent applications from blocking NMI. 0 - Host interrupt blocking disabled 1 - Host interrupt blocking enabled
29	R/W	vsb	This bit selects the capture address range for SoundBlaster access. 0 - Address range : 220xH - 22FxH 1 - Address range : 240xH - 24FxH
28:27	R/W	vmpu[1:0]	These bits select the capture address range for the Base Register. 00 - Address range : 320xH - 327xH 01 - Address range : 330xH - 337xH 10 - Address range : 340xH - 347xH 11 - Address range : 350xH - 357xH
26:25	R/W	vcdc[1:0]	These bits select the capture address range for the CODEC. 00 - Address range : 530xH - 537xH 01 - Undefined 10 - Address range : E80xH - E87xH 11 - Address range : F40xH - F47xH
24	R/W	firq	This bit is used to force an interrupt. 0 - Do not force an

interrupt 1 - Force an interrupt
23 R/W sdmacap This bit enables event capture for the Slave DMA Controller. The decoded address range for this event is C0xH - DFxH. 0 - Disables event capture 1 - Enables event capture
22 R/W spicap This bit enables event capture for the Slave Interrupt Controller. The decoded address range for this event is A0xH - A1xH. 0 - Disables event capture 1 - Enables event capture
21 R/W mdmacap This bit enables event capture for the Master DMA Controller. The decoded address range for this event is 0xH - FxH. 0 - Disables event capture 1 - Enables event capture
20 R/W mpicap This bit enables event capture for the Master Interrupt Controller. The decoded address range for this event is 20xH - 21xH. 0 - Disables event capture 1 - Enables event capture
19 R/W adcap This bit enables event capture for the ADLIB registers . The decoded address range for this event is 388xH - 38BxH. 0 - Disables event capture 1 - Enables event capture
18 R/W sbcap This bit enables event capture for the SoundBlaster registers. The decoded address range for this event is selected by the VSB control bit. 0 - Disables event capture 1 - Enables event capture
17 R/W cdccap This bit enables event capture for the CODEC. The decoded address range for this event is selected by the VCDC[1:0] control bits. 0 - Disables event capture 1 - Enables event capture
16 R/W bacap This bit enables event capture for the SoundScape Base Address register. The decoded address range for this event is selected by the VMPU[1:0] control bits. 0 - Disables event capture 1 - Enables event capture
15:11 R one These bits will always read back as ones
10:8 R e2, e1, e0 These three bits are the event number of the captured event. The event number corresponds to the enable bit which allowed the interrupt. Their decoding is shown below: 000 - SoundScape Base Address 001 - CODEC 010 - SoundBlaster Registers 011 - ADLIB Registers 100 - Master Interrupt Controller 101 - Master DMA Controller 110 - Slave Interrupt Controller 111 - Slave DMA Controller
7:3 R a[4:0] These bits are the least significant I/O address bits during the event captured.
2 R w/r This bit indicates whether the event captured was a read or write operation. 0 - Event captured was a Read 1 - Event captured was a Write
1 R zero This bit always reads back as a zero.
0 R/W int# This bit is the interrupt flag for LEGACY events. A write to this bit (0 or 1) resets the interrupt flag. 0 - Interrupt did occur 1 - Interrupt did not occur

7.7. Channel Status Block {S/PDIF}

There is 1user accessible 32 bit channel Status register in the channel status block. The 32 bit control register can be read or written.

For more details into the use of the available options in S/PDIF {Sony/Phillips Digital Interface}, we recommend that the user look into the IEC958 spec, which details the timing for the S/PDIF ports on this chip.

Channel Status Control Register Address 1CH
Addressable as byte, word, longword

Power on reset value C0200004H Direct Mapped

Bit(s) R/W Name Function

31:30 R/W RESERVED .

29:28 R/W Clock Accuracy These bits are used to select the S/PDIF clock accuracy. 00 - level II, normal accuracy mode 10 - variable pitch shifted clock mode 01 - level I, high accuracy mode

27:24 R/W Sample Rate These bits are used to select the S/PDIF sample rate. 0000 - 44.1KHz sampling frequency *(NOT SUPPORTED!)* **0010 - 48KHz sampling frequency** *(ONLY RATE WE SUPPORT!)* 0011 - 32KHz sampling frequency *(NOT SUPPORTED!)*

23:19 R/W Channel Number These bits are used to select the source number. 0000 - don't care 0001 - A 0010 - B 0011 - C … all the way to 1111 - O

18:16 R/W SOURCE Number These bits are used to select the S/PDIF source number. 0000 - don't care 0001 - 1 0010 - 2 0011 - 3 … all the way to 1111 - 15

15 R/W L This bit is used for copy protection purposes only. Category codes 001X XXX, 01111 XXX, 100X XXX 0 - Original commercial prerecorded data (digital copying prohibited) 1 - No indication of 1st generation or higher (digital copying permitted) All other category codes 0 - No indication of 1st generation or higher (digital copying permitted) 1 - Original commercial prerecorded data (digital copying prohibited)

14:8 R/W Category Code Category code. 000 0000 - General 100 0000 - Experimental xxx 0000 - Reserved xxx 1000 - Solid State Memory xxx x100 - Broadcast Reception of Digital Audio xxx x010 - Digital/Digital converters and signal processing xx0 0110 - A/D converters without copyright xx1 0110 - A/D converters with copyright (using Copy and L) xxx 1110 Broadcast reception of digital audio xxx x001 - Laser Optical xxx x101 - Musical Instruments, mics etc. xxx x011 - Magnetic Tape or Disk xxx x111 - reserved

7:6 R/W Mode mode = 00, all other states reserved

5:3 R/W EMPHASIS If bit 1 = 0 (digital audio) 000 - 2 audio channels without pre-emphasis 001 - 2 audio channels with 50/15usec pre-emphasis 010 - reserved 2- channel audio 011 - reserved 2 channel audio 1xx - reserved 4 channel audio If bit 1 = 1 (non audio) 000 - digital data - all other states are reserved

2 R/W COPY This bit selects Copy Prohibit state 0 - Copy Prohibited/copyright material 1 - Copy Permitted, copyright not asserted - default

1 R/W AUDIO_0 0 - Digital Audio - default 1 - Non Audio

0 R/W PRO_0 This bit identifies block as AES consumer format. 0 - S/PDIF { Only Legal value}

7.8. Serial Interface

There is one 16 bit control register and three 32 bit control/status registers in the serial block. The 16 bit control register can be read or written. The three 32 bit control/status registers can be read or written but only the lower 16 bits can actually be written. The upper 16 bits of these registers provides the status of the internal sample counter.

Serial Interface Control Register Address 20H

Addressable as byte, word, longword

Power on reset value FF800000H Direct Mapped

Bit(s) R/W Name Function

31:23 R/W ONES These bits always read back as ones. They are not writable.

22 R/W DAC_TEST This bit is used for testing purposes. It will select the I2S lrclk input signal as the source for the playback and record channels. It is used for test vector generation purposes only. 0 - DAC test mode disabled. 1 - DAC test mode enabled.

21:19 R/W p2_end_inc[2:0] These bits are the binary offset value that will be added to the sample address counter at the end of the loop. This value is used only if the DAC2 channel is in loop mode; it is not used in stop mode. If loop mode is selected this value must be greater than zero otherwise the channel will not function correctly. This minimum value will be one if 8 bit mode is selected and two if 16 bit mode is selected.

18:16 R/W p2_st_inc[2:0] These bits are the binary offset value that will be added to the

sample address counter when the channel is started/restarted. This value can be zero and will allow the sample fetch to start on any byte boundary. For 16 bit data this value must be an even number.
15 R/W r1_loop_sel This bit selects loop/stop mode for the ADC channel. This bit determines what action the channel will perform when the sample count reaches zero. 0 - Loop mode ; interrupt set (if enabled) but keeps recording 1 - Stop mode ; interrupt set (if enabled) , stops recording
14 R/W p2_loop_sel This bit selects loop/stop mode for the DAC2 channel. This bit determines what action the channel will perform when the sample count reaches zero. 0 - Loop mode ; interrupt set (if enabled) but keeps playing 1 - Stop mode ; interrupt set (if enabled) , plays last sample
13 R/W p1_loop_sel This bit selects loop/stop mode for the DAC1 channel. This bit determines what action the channel will perform when the sample count reaches zero. 0 - Loop mode ; interrupt set (if enabled) but keeps playing 1 - Stop mode ; interrupt set (if enabled) , plays last sample
12 R/W p2_pause This bit selects pause mode for the DAC2 playback channel. When in pause mode the channel will playback the last sample. 0 - Play mode ; normal playback mode or removes channel from pause mode on next sample after bit is cleared 1 - Pause mode ; plays last sample continuously on next sample after the pause bit has been set
11 R/W p1_pause This bit selects pause mode for the DAC1 playback channel. When in pause mode the channel will playback the last sample. 0 - Play mode ; normal playback mode or removes channel from pause mode on next sample after bit is cleared 1 - Pause mode ; plays last sample continuously on next sample after the pause bit has been set
10 R/W r1_int_en This bit is the interrupt enable bit for the ADC channel. To clear the interrupt this bit must be set to zero and then set to one to enable the next interrupt. 0 - ADC interrupt disabled 1 - ADC interrupt enabled
9 R/W p2_intr_en This bit is the interrupt enable bit for the DAC2 channel. To clear the interrupt this bit must be set to zero and then set to one to enable the next interrupt. 0 - DAC2 interrupt disabled 1 - DAC2 interrupt enabled
8 R/W p1_intr_en This bit is the interrupt enable bit for the DAC1 channel. To clear the interrupt this bit must be set to zero and then set to one to enable the next interrupt. 0 - DAC1 interrupt disabled 1 - DAC1 interrupt enabled
7 R/W p1_sct_rld This bit when set high will force the sample counter for DAC1 to be reloaded with the sample count register value on the next rising edge of the DAC1 left/right clock. This bit can be returned low on the following instruction. It does not have to be held high for more than 1 microsecond. This control bit is rising edge triggered.
6 R/W p2_dac_sen This bit when set high will enable the DAC2 to continue playback when it is in the stopped condition and the DAC2 channel has been disabled. Without this bit set if the DAC2 channel is disabled it will begin to playback zeros. 0 - DAC2 plays back zeros when disabled 1 - DAC2 plays back last sample when disabled and in stop mode
5:4 R/W r1_s_eb : r1_s_mb These two bits select the data format for the ADC channel. For eight bit data modes the msb is always inverted before it is written out to the buffer. For mono modes only the left channel data is recorded. 00 - Eight bit - Mono mode 01 - Eight bit - Stereo mode 10 - Sixteen bit - Mono mode 11 - Sixteen bit - Stereo mode
3:2 R/W p2_s_eb : p2_s_mb These two bits select the data format for the DAC2 channel. For eight bit data modes the msb is always inverted after it is read from the buffer. For mono modes the left channel data is duplicated for both the left and right channels. 00 - Eight bit - Mono mode 01 - Eight bit - Stereo mode 10 - Sixteen bit - Mono mode 11 - Sixteen bit - Stereo mode
1:0 R/W p1_s_eb : p1_s_mb These two bits select the data format for the DAC1 channel. For eight bit data modes the msb is always inverted after it is read from the buffer. For mono modes the left channel data is duplicated for both the left and right channels. 00 - Eight bit - Mono mode 01 - Eight bit - Stereo mode 10 - Sixteen bit - Mono mode 11 - Sixteen bit - Stereo mode

DAC1 Channel Sample Count Register Address 24H

Addressable as word, longword

Power on reset value 00000000H Direct Mapped

Bit(s) R/W Name Function

31:16 R curr_samp_ct These bits are the current value of the internal sample counter for the DAC1 playback channel. The number of samples that have been played is samp_ct - curr_samp_ct.

15:0 R/W samp_ct These bits are the number of samples minus one that the DAC1 channel will playback.

DAC2 Channel Sample Count Register Address 28H

Addressable as word, longword

Power on reset value 00000000H Direct Mapped

Bit(s) R/W Name Function

31:16 R CURR_SAMP_CT These bits are the current value of the internal sample counter for the DAC2 playback channel. The number of samples that have been played is samp_ct - curr_samp_ct.

15:0 R/W samp_ct These bits are the number of samples minus one that the DAC2 channel will playback.

ADC Channel Sample Count Register Address 2CH

Addressable as word, longword

Power on reset value 00000000H Direct Mapped

Bit(s) R/W Name Function

31:16 R curr_samp_ct These bits are the current value of the internal sample counter for the ADC record channel. The number of samples that have been played is samp_ct - curr_samp_ct.

15:0 R/W samp_ct These bits are the number of samples minus one that the ADC channel will record.

7.9. Host Interface - Memory

The top 64 bytes of memory are actually used as register storage for the CCB block and also as the FIFO for the UART block. The CCB registers are located in the lower 32 bytes of this block and require six longwords. These registers control filling the circular buffers for the two playback channels and the record channel. Each channel requires 2 longwords. The UART FIFO is located in the upper 32 bytes of this block and requires all eight longwords but uses only 9 bits of each longword.

DAC1 Frame Register 1 Address 30H

Addressable as longword Memory Page 1100b

Power on reset value xxxxxxxxH Direct Mapped

Bit(s) R/W Name Function

31:0 R/W PCI address This longword is the physical PCI address of DAC1 sample buffer in system memory

DAC1 Frame Register 2 Address 34H

Addressable as longword Memory Page 1100b

Power on reset value xxxxxxxxH Direct Mapped

Bit(s) R/W Name Function

31:16 R/W Current Count This 16 bit counter indicates the number of longwords that have been transferred.

15:0 R/W Buffer Size This 16 bit value indicates the number of longwords in a buffer minus one.

DAC2 Frame Register 1 — Address 38H

Addressable as longword — Memory Page 1100b
Power on reset value xxxxxxxxH — Direct Mapped

Bit(s)	R/W	Name	Function
31:0	R/W	PCI address	This longword is the physical PCI address of DAC2 sample buffer in system memory

DAC2 Frame Register 2 — Address 3CH

Addressable as longword — Memory Page 1100b
Power on reset value xxxxxxxxH — Direct Mapped

Bit(s)	R/W	Name	Function
31:16	R/W	Current Count	This 16 bit counter indicates the number of longwords that have been transferred.
15:0	R/W	Buffer Size	This 16 bit value indicates the number of longwords in a buffer minus one.

ADC Frame Register 1 — Address 30H

Addressable as longword — Memory Page 1101b
Power on reset value xxxxxxxxH — Direct Mapped

Bit(s)	R/W	Name	Function
31:0	R/W	PCI address	This longword is the physical PCI address of ADC sample buffer in system memory

ADC Frame Register 2 — Address 34H

Addressable as longword — Memory Page 1101b
Power on reset value xxxxxxxxH — Direct Mapped

Bit(s)	R/W	Name	Function
31:16	R/W	Current Count	This 16 bit counter indicates the number of longwords that have been transferred.
15:0	R/W	Buffer Size	This 16 bit value indicates the number of longwords in a buffer minus one.

UART FIFO Register — Address 30, 34, 38, 3CH

Addressable as longword — Memory Pages 1110, 1111b
Power on reset value xxxxxxxxH — Direct Mapped

Bit(s)	R/W	Name	Function
31:9	R/W	open	These bits are not used.
8	R/W	byte valid	This bit indicates whether the UART byte contains valid data. 0 - UART byte not valid 1 - UART byte valid
7:0	R/W	UART byte	This byte is a byte the has been received by the UART block through the MIDI interface.

8. POWER MANAGEMENT

All power management of the system is under software control. The AC97 CODEC and AudioPCI 97 can be powered down separately. Neither chip loses register information when powered down.
The AudioPCI 97 can be power managed by shutting down various sub-systems. The following blocks can be individually powered down: Joystick, UART, and Serial Interface. Although these blocks can be individually disabled this will not save an appreciable amount of power. AudioPCI 97 can also individually internally shut down the PCI clock and the Crystal input clock. The PCI clock when shut down will still be active to the PCI and Interrupt/Chip Select modules. The Crystal clock when shut down will be shut down for all internal modules as well as the output connection to the AC97 CODEC.
During operation, the AudioPCI 97 ASIC will have a typical power dissipation of 150mW. In power down, the AudioPCI 97 ASIC will have a typical power dissipation of 15mW.

8.1. CODEC Power Management

The AC97 CODEC's are powered down by setting bit 1 (of control bits 7 - 0) in control register 16 (hex) to a zero. The AC97 CODEC control registers are written through the CODEC Interface block at address 14 (hex). For details refer to the AC97 specification and also the CODEC Interface section (7.5) of this specification.

8.2. AUDIOPCI Power Management

As mentioned above, the Joystick, UART, and Serial Interface modules of the AudioPCI 97 chip can be individually powered down. The remaining modules will be in a powered up condition. The AudioPCI 97 modules are powered down by setting bits 6 - 2 (of control bits 31 - 0) to zero. The AudioPCI 97 control register is located in the IRQ and Chip Select Block at address 00 (hex). For details refer to the IRQ and Chip Select Block section (7.1) of this specification. Note that the Serial Interface actually has three separate enable bits, one for each of the playback channels and one for the record channel.
Although these blocks can be individually disabled this will not save an appreciable amount of power. AudioPCI 97 can also individually internally shut down the PCI clock and the Crystal input clock. The PCI clock when shut down will still be active to the PCI and Interrupt/Chip Select modules. The Crystal clock when shut down will be shut down for all internal modules as well as the output connection to the AC97 CODEC.

9. PCI BUS Description and Signals

AudioPCI 97 is designed to adhere to the PCI Local Bus Specification Revision 2.2, as such it complies with all requirements for bus master capability. It is a 32 bit device and does not currently support the optional 64 bit bus modes. Of the optional pins described in the PCI specification, AudioPCI 97 only uses Interrupts.
Although the Sample buffer space is referred to as cache, it is not the system memory cache described in the PCI specification. This cache is a local sound memory cache and is not part of the directly accessible system memory. **Note:** The "#" symbol indicates a low active signal.

9.1. Parity

AudioPCI 97 implements the PAR signal. This signal is an even parity check described in the PCI specification. AudioPCI 97 will generate PAR whenever it drives AD[31:0]. Although AudioPCI will generate PAR , it will not generate the Bus Error condition signals PERR# and SERR# due to parity errors on data received. This exception is allowed in the PCI Specification section 3.8.2.

9.2. LOCK#

AudioPCI 97 does not support PCI bus lock functions.

9.3. Bus Speed

Since AudioPCI 97 uses a high speed intermediate buffer to transfer data to and from the PCI bus, it runs at the standard 33 MHz. Rate. However, it is believed that the memory speed on the PCI bus may limit the transaction rate by inserting one wait state. All latency calculations are based on this assumption.

10. PIN DESCRIPTION

10.1. PCI Interface

The PCI Interface follows the information presented on the PCI Local Bus Specification Revision 2.2. For a more complete description of each of the PCI signal please refer to the PCI specification.

CLK Clock: A 33MHz input signal from the PCI bus. This is the master timing control for all PCI transfers.

RST# Reset: The device will essentially be in sleep mode after reset.

AD[31:0] Address/Data: multiplexed signals of the PCI Bus.

C/BE#[3:0] Bus Command and Byte Enables: Defines the type of transfer that will take place.

FRAME# Cycle Frame: Driven by the current bus master, this signal indicates the beginning of a transfer. When FRAME# is de-asserted, the transaction is in the final phase.

IRDY# Initiator Ready: This signal indicates that the initiating agent (the bus master) is able to accept the data phase of the transaction. Normally used to create wait states by the master.

TRDY# Target Ready: Driven by the target (the selected device), this signal indicates that the target is ready for the data transaction. Generally used to generate wait states by the target.

STOP# Stop: indicates the current target is requesting the master to stop the current transaction.

PAR Parity signal is even parity. The number of “1”s on AD[31:0],C/BE[3:0] and Par equal an even number.

IDSEL Initialization Device Select: This signal is used as a chip select during configuration read and write transactions

DEVSEL# Device Select: This signal, when actively driven, indicates that the driving device has decoded its address as the target of the current transaction.

REQ# Request: indicates to the arbiter that ES1380 desires use of the bus.

GNT# Grant: This signal indicates that control of the PCI Bus has been granted and ES1380 is now the bus master.

INTA# Interrupt A: ES1380 supplies interrupt support for all possible interrupt configurations. This is done so that the greatest possible flexibility can be achieved during the configuration process.

SERR# This pin is implemented for NMI

10.2. AC97 CODEC Interface {AC_LINK}.

SYNC AC97 CODEC 48KHz Fixed Rate Sample Sync output to CODEC.

BCLK AC97 CODEC Shift {Bit}Clock input from CODEC. {12.288MHz}

SDATA_IN AC97 CODEC TDM Receive data input from CODEC.

SDATA_OUT AC97 CODEC TDM Transmit data output to CODEC.

10.3. AC97 Specific Pins

XTALI 24.576MHz Crystal input. Used to generate AC97CODEC Master Clocks.

XTALO Crystal output.
XTALO_BUF Buffered Crystal Output to AC_97 CODEC Master Clock input
GPIO[3:0] General Purpose Input/Output pins. These pins can be programmed to be either inputs or outputs. These are tied to the AC97 subsystem. They have internal pull-ups.

10.4. Miscellaneous Pins

MIDI In UART serial or MIDI In from outside world MIDI device
MIDI Out UART serial output for MIDI out to outside world MIDI device
Joystick Axis Dual Joystick Axis control inputs
Joystick Buttons Dual Joystick Pushbutton inputs

S_OUT_BCLKI S/PDIF compatible digital output., or I2S BCLK Input
S_THRU_I2S_I S/PDIF_THRU or I2S SERIN
S/PDIF Mode:
Input to digital output mux which selects between
internal S/PDIF data or signal at this input (allows pass-through of S/PDIF data).

I2S_Mode:
Serial Digital Audio Data input

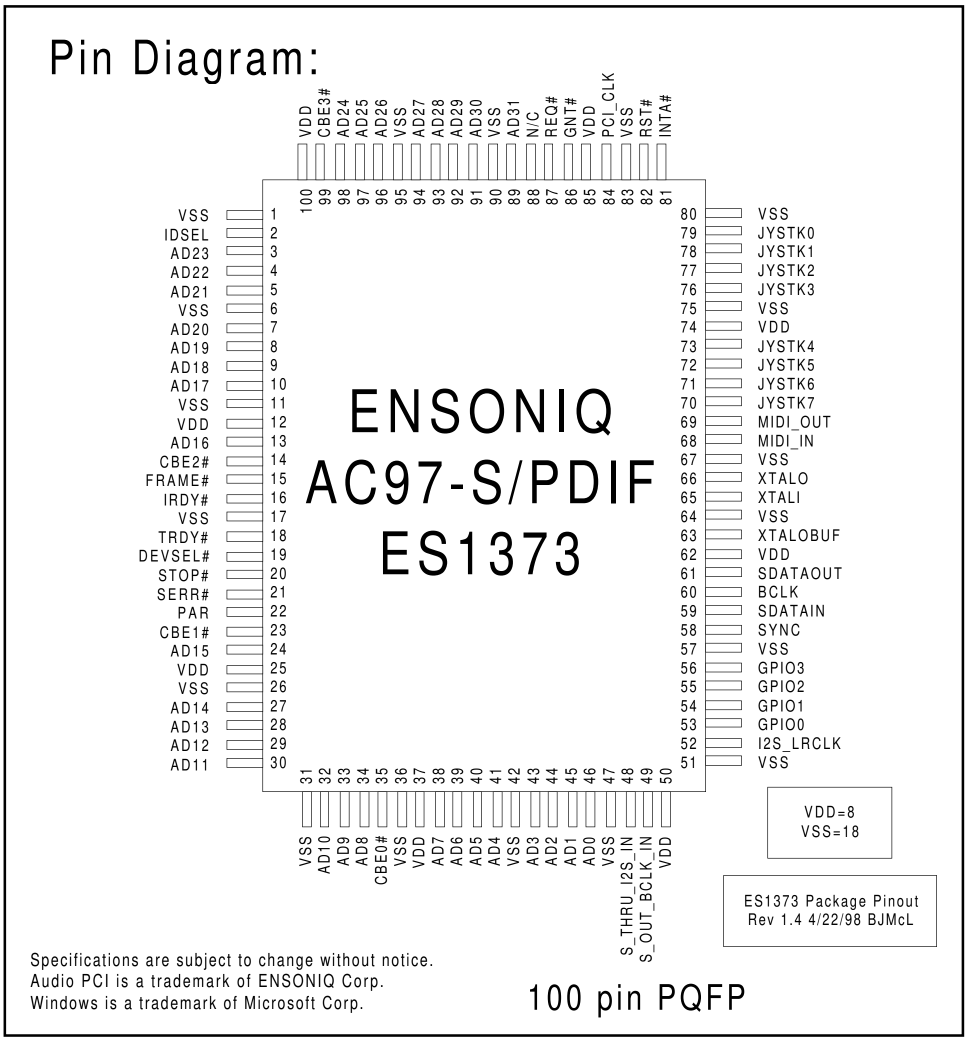
I2S_LRCLKIN I2S Left/Right clock input.

Power Supplies:
VDD Digital Supply Voltage (+5v)
VSS Digital Ground pins

11. PINLIST

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	VSS	31	VSS	51	VSS	81	INTA#
2	IDSEL	32	AD10	52	I2S_LRCLK_IN	82	RST#
3	AD23	33	AD09	53	GPIO0	83	VSS
4	AD22	34	AD08	54	GPIO1	84	CLK
{PCI}							
5	AD21	35	C/BE0#	55	GPIO2	85	VDD
6	VSS	36	VSS	56	GPIO3	86	GNT#
7	AD20	37	VDD	57	VSS	87	REQ#
8	AD19	38	AD07	58	SYNC	88	N/C
9	AD18	39	AD06	59	SDATAIN	89	AD31
10	AD17	40	AD05	60	BCLK	90	VSS
11	VSS	41	AD04	61	SDATAOUT	91	AD30
12	VDD	42	VSS	62	VDD	92	AD29
13	AD16	43	AD03	63	XTALOBUF	93	AD28
14	C/BE2#	44	AD02	64	VSS	94	AD27
15	FRAME#	45	AD01	65	XTALI	95	VSS
16	IRDY#	46	AD00	66	XTALO	96	AD26
17	VSS	47	VSS	67	VSS	97	AD25
18	TRDY#	48	S_THRU_I2S_IN	68	MIDI_IN	98	AD24
19	DEVSEL#	49	S_OUT_BCLK_IN	69	MIDI_OUT	99	C/BE3#

20	STOP#	50	VDD	70	JYSTK7	100	VDD
21	SERR#			71	JYSTK6		
22	PAR_OUT			72	JYSTK5		
23	CBE1#			73	JYSTK4		
24	AD15			74	VDD		
25	VDD			75	VSS		
26	VSS			76	JYSTK3		
27	AD14			77	JYSTK2		
28	AD13			78	JYSTK1		
29	AD12			79	JYSTK0		
30	AD11			80	VSS		



12. TIMING.

AudioPCI 97 is being designed to conform to the PCI Local Bus Specification Revision 2.2

For detailed information on the PCI timing for AudioPCI 97 please refer to section 3.3 Bus Transactions in the PCI Specification.

The timing information for the signals from the AudioPCI 97 to the AC97 CODEC can be found in the Audio Codec '97 Component Specification.

13. Electrical Characteristics

13.1.1 Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Unit
Power supplies: Digital	VDD	4.75	5.0	5.25	V
Power Supply Current (estimated)			**100**	**125**	ma

Normal Operation Digital - D3 Standby Mode Digital - D2 Suspend Mode Digital - D1 Low Power Mode Digital - D0

Digital Input Voltage

Storage temperature

13.1.2 Absolute Maximum Ratings

Parameter	Symbol	min	typ	max	Unit
Power supplies: Digital	VDD	-0.5		4	V
Power Supply Current Normal Operation. Power Down TBD	ma ua	ICC			TBD
Digital Input Voltage		-0.5		6	V

Storage temperature	-40	125	^{0}C

13.1.3 Recommend Operating Conditions

(DGND = 0V, all voltages with respect to 0V.)

Parameter	**Symbol**	**min**	**typ**	**max**	**Unit**
Power supplies: Digital	VDD	3.0	3.3	3.6	V
Operating ambient temperature	T_A	0	25	70	^{0}C

13.1.4 DC Characteristics - Digital

(Conditions: T_A=0 ~ 70 ^{0}C, VDD=3.0 to 3.6v)

ALL PCI pads must conform to 'universal' PCI rev 2.2 specification and "5v tolerant"

Parameter	**Symbol**	**Condition**	**min**	**max**	**unit**	
TTL Type						
Low Level Output Voltage	VOL			0.4	V	
High Level Output Voltage	VOH		2.4		V	
Low Level Input Voltage	VILTTL			0.8	V	
High Level Input Voltage	VIHTTL		2.0		V	
Low Level Input Current	IIL			10	uA	
High Level Input Current	IIH			10	uA	
Input Leakage Current		0<Vin<Vcc		+/- 5	uA	
Output Z-State Leakage Current		0<Vout<Vcc		+/- 5	uA	
High Level Output Current 12mA 8 mA pad 4 mA pad 4	mA mA mA		|IOH|	VOH=min		12 8
Low Level Output Current 12mA 8 mA pad 4 mA pad 4	mA mA mA		|IOL|	VOL=max		12 8

13.1.4.1 DC Specifications for 5V signaling

(Conditions: T_A=0 ~ 70 ^{0}C, VDD=4.5 to 5.5v)

ALL PCI pads must conform to 'universal' PCI rev2.2 specification and "5v tolerant". It is the responsibility of the ASIC vendor to devise an appropriate combination of device characterisation and production tests ,in order to guarantee the PCI components complies with the design definition in PCI rev2.2 .

Parameter	**Symbol**	**Condition**	**min**	**max**	**unit**	**Notes**
PCI Type						
PCI Supply Voltage	Vdd		4.75	5.25	V	
Input High Voltage	Vih		2.0	Vcc+0.5	V	
Input Low Voltage	Vil		-0.5	0.8	V	
Low Level Output Voltage	VOL	Iout=3,6mA		0.55	V	2
High Level Output Voltage	VOH	Iout=-2mA	2.4		V	
Input Low Leakage Current	Iil	Vin=0.5		-70	uA	1
Input High Leakage Current	Iih	Vin=2.7		70	uA	1
Input Pin Capacitance	Cin			10	pF	

PCI CLK Pin Capacitance	Cclk		5	12	pF	
PCI IDSEL Pin Capacitance	Cidsel			8	pF	
Pin Inductance	Lpin			20	nH	3

13.1.4.2 DC Specifications for 3.3V signaling

(Conditions: T_A=0 ~ 70 ^{0}C, VDD=3.0 to 3.6v)

ALL PCI pads must conform to 'universal' PCI rev2.2 specification and "5v tolerant". It is the responsibility of the ASIC vendor to devise an appropriate combination of device characterization and production tests ,in order to guarantee the PCI components complies with the design definition in PCI rev2.2 .

Parameter	**Symbol**	**Condition**	**min**	**max**	**unit**	**Notes**
PCI Type						
PCI Supply Voltage	Vdd		3.0	3.6	V	
Input High Voltage	Vih		0.5Vcc	Vcc+0.5	V	
Input Low Voltage	Vil		-0.5	0.3Vcc	V	
Input Pull-up Voltage	Vipu		0.7Vcc		V	
Low Level Output Voltage	VOL	Iout=1.5mA		0.1Vcc	V	
High Level Output Voltage	VOH	Iout=-500uA	0.9Vcc		V	
Input Leakage Current	Iil	0<Vin<Vcc		+/- 10	uA	1
Input Pin Capacitance	Cin			10	pF	
PCI CLK Pin Capacitance	Cclk		5	12	pF	
PCI IDSEL Pin Capacitance	Cidsel			8	pF	
Pin Inductance	Lpin			20	nH	3

Notes:

1? Input leakage current include hi-Z output leakage for all bi-directional buffers with tri-state outputs.

2? Signal without pull-up resistors must have 3mA low output current. Signals requiring pull-up must have 6mA.

13.1.5 AC Characteristics - Digital

(T_A=0~70 ^{0}C, VCC=4.5 to 5.5v)

Symbol	**Parameter**	**min**	**typ**	**max**	**unit**
PCICLK	PCI clock frequency duty cycle	45%	33.0	55%	MHz
XTALI	Xtal clock frequency duty cycle	45%	24.576	55%	Mhz

13.1.5.1 AC Specifications for 5V signaling

Parameter	**Symbol**	**Condition**	**min**	**max**	**unit**	**Notes**
PCI Type						
Switching Current HIGH	Ioh	0<Vout<=1.4	-44		mA	
		1.4<Vout<2.4	-44+(Vout-1.4)/0.024		mA	
		3.1<Vout<Vcc		Eqt's A		

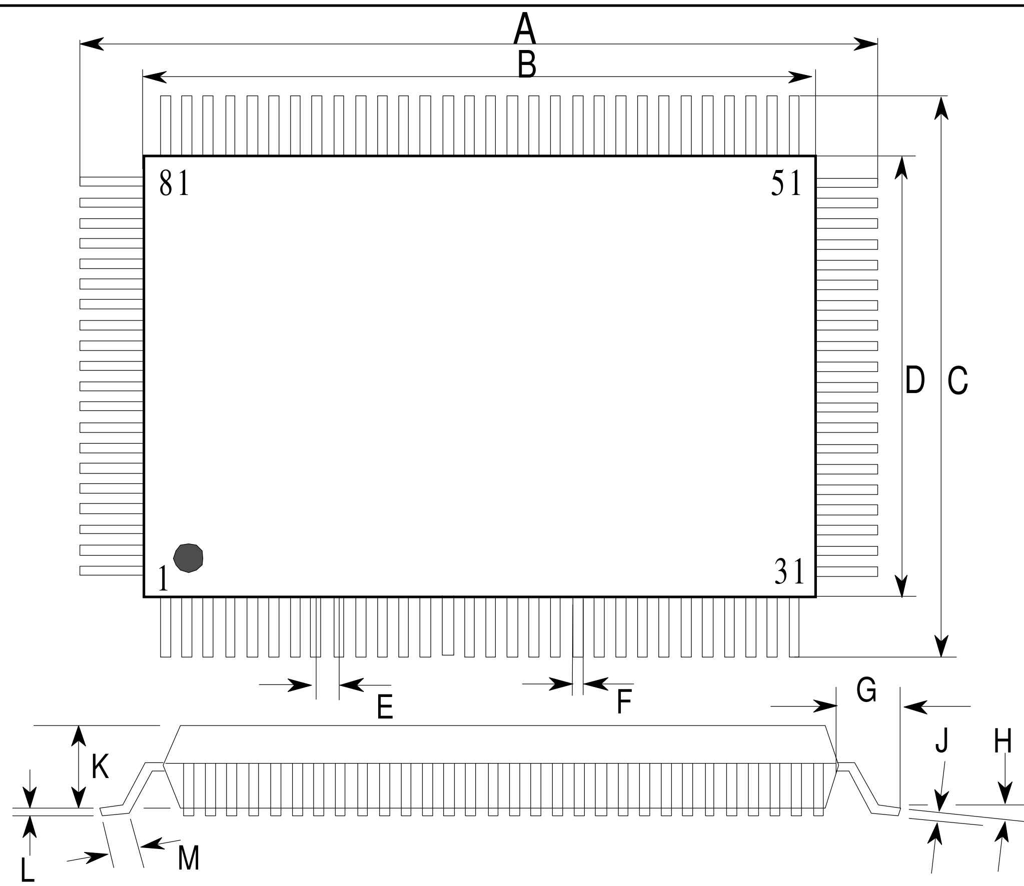
Test Point		Vout=3.1		-142	mA	
Switching Current LOW	Iol	Vout>=2.2	95		mA	
		2.2>Vout>0.55	Vout/0.023		mA	
		0.71>Vout>0		Eqt's B		
Test Point		Vout=0.71		206	mA	
Low Clamp Current	Icl	-5<Vin<-1	-25+(Vin+1)/0.015		mA	
Output Rise Slew Rate	SlewR	0.4V - 2.4V Load		1	5	V/ns
Output Fall Slew Rate	SlewF	2.4V - 0.4V Load		1	5	V/ns

13.1.5.2 AC Specifications for 3.3V signaling

Parameter	**Symbol**	**Condition**	**min**	**max**	**unit**	**Notes**
PCI Type						
Switching Current HIGH	Ioh	0<Vout<=0.3Vdd	-12Vdd		mA	
		0.3Vdd<Vout<0.9Vdd	-17.1(Vdd-Vout)		mA	
		0.7Vdd<Vout<Vdd		Eqt's C		
Test Point		Vout=0.7Vdd		-32Vdd	mA	
Switching Current LOW	Iol	Vout>=2.2	16Vdd		mA	
		Vdd>Vout>0.6Vdd	26.7Vout		mA	
		0.6Vdd>Vout>0		Eqt's D		
Test Point		Vout=0.18Vdd		38Vdd	mA	
Low Clamp Current	Icl	-3<Vin<-1	-25+(Vin+1)/0.015		mA	
Output Rise Slew Rate	SlewR	0.2Vdd - 0.6Vdd Load		1	4	V/ns
Output Fall Slew Rate	SlewF	0.6Vdd - 0.2Vdd Load		1	4	V/ns

Notes: Refer to the V/I curves and test conditions specified in PCI specification Rev2.2

14. Mechanical Information



100 Pin QFP Plastic Package

	MILLIMETERS			
DIM	MIN	NOM	MAX	Note
A	23.65	23.90	24.15	
B	19.90	20.00	20.10	
C	17.65	17.90	18.15	
D	13.90	14.00	14.10	
E	0.65	0.65	0.65	
F	0.20	0.30	0.40	
G	1.95	1.95	1.95	
H	0 TO 10 Degree's			
J	0.15	0.15	0.15	
L	0.10	0.25	0.40	
K	2.57	2.72	2.87	

15. APPENDIX

15.1. Bus Latency

Since each audio channel has a 64 byte buffer, the Latency requirement for the PCI bus can be calculated as follows:

For 8 bit audio: 32 Samples (one half buffer) @ 44.1 kHz. = 725µsec.
For 16 bit audio: 16 Samples @ 44.1 kHz. = 363 µsec.

Therefore, once a Bus Request is made, AudioPCI 97 needs to have the PCI bus grant in 363 µsec. for 16 bit samples. In most game environments the sound effects are 8 bit and the high latency figure is acceptable. If more than one channel needs servicing, this does not impact the latency calculation because once the PCI Bus is granted it can be held until all channels are serviced. Since AudioPCI 97 uses 8 Long Word burst transfers, each channel is filled with one burst transfer and AudioPCI 97 can service all three with just 24 transfers.

15.2. Bus Bandwidth

The Bus bandwidth required by AudioPCI is very low. If all three channels are running at 44.1 kHz the total bandwidth is:

44.1 kHz $\times$ 2 (stereo) $\times$ 3 (channels) $\times$ 2 (bytes) = 529 KBytes/sec.

This represents less than 0.5% of the available PCI Bus bandwidth.

16. SPEC REVISION HISTORY

This section details the changes that have been made to this living document.

Rev	Date	Description:
1.0		
1.1		
1.2		
1.3	2-15-98	Changed PME# pin documentation. • Removed PME# pin description (page 31). • Changed PME# pin to an NC on the pinout (page 33). • Added notes that PME# pin not implemented on ES1371 in PMC configuration register description in the PCI Configuration Space (page 13).
1.4	3-03-98	Revised Block Diagram to show connection between SRC and Serial Block. Fixed address ranges in the Legacy Control/Status Register (page 22).
1.5	4-22-98	Added Electrical characteristics section and revised Package Drawing
1.6	5-11-98	Added new register bits for GPIO interrupts
1.7	5-12-98	Added Subsystem ID and Subsystem Vendor ID programming info.
1.8	5-28-98	Fixed ENABLE_SPDIF sense.